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EXAMINER
TAHA, SHAQ

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/518,930	**Applicant(s)** KOISTINEN ET AL.	
	Examiner SHAQ TAHA	**Art Unit** 2446	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 January 2009_.

2a)☒ This action is **FINAL**. 2b)□ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _26 - 37 and 41 - 57_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _26 - 37 and 41 - 57_ is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)□ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) □ Notice of Informal Patent Application

6) □ Other: _____.

DETAILED ACTION

This is a final action for application number 10/518,930 based on after non-final filed on 11/20/2007. The original application was filed on 12/27/2004. Claims 26 – 37, 41 - 56 are currently pending and have been considered below. Claims 26, 41, 50, 51, 52, 53, and 54 are independent claims.

Applicant's Response

Applicant's arguments filed in the amendment filed 01/28/09, have been fully considered but they are not persuasive. The reasons are set forth below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26 – 37, 41 – 47, and 49 - 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaniyar et al. (US 2003/0187914) in view of Aviani et al. (US 6,976,085)

Regarding claims 26 and 52, Kaniyar et al. teaches a method, comprising: obtaining a current connection state as well as a current load state of each of a plurality of processors configured to perform communication in a packet switched connection, **[After the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests, wherein before choosing one of the processors to handle a request as shown in Fig. 3a, the load-balancing multiprocessor will obtain a connection state of the processors and the load state of the processors to send the request to the connected and least busy processor, (Kaniyar et al., Paragraph 31, Page 3)],**

selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processors irrespective of a specific connection to which this next received packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

and maintaining information about the load state of each processor so that said selecting is performed by selecting one of said processors to serve and process a respective received packet based on the load state, **[A scheduling processor in the multiprocessor system, selected by a load-balancing algorithm, reads each data packet and applies a mapping algorithm to portions of the data packet yielding a**

map value, wherein the interrupt request rotates between the available processors on a round-robin basis so that the multiprocessor system will maintain information regarding the load and connection state of the processors, (Kaniyar et al., Paragraph 8, Page 1)],

Kaniyar et al. fails to teach informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 27, a method wherein said data storage is accessed by said load balancer, **[magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store the desired information and which can be accessed by the SMP systems as shown in Fig. 2, (Kaniyar et al., Paragraph 28, Page 3)].**

Regarding claim 28, a method wherein said data storage is accessed by said processors, **[SMP systems 100a-b include two or more processing units 250a-b, communication device(s) 225 and memory 240 as shown in Fig. 2, (Kaniyar et al., Paragraph 27, Page 3)].**

Regarding claim 29, a method wherein said information about the load state is maintained as a Boolean state, **[it is inherent to use a Boolean value, since it is a digital or analog that depends on 1s and 0s, or true and false].**

Regarding claim 30, a method wherein a processor is selected in a round-robin fashion, **[the interrupt request rotates between the available processors on a round-robin basis, (Kaniyar et al., Paragraph 31, Page 3].**

Regarding claim 31, a method wherein a supported service profile for each unit processor is maintained, **[The NIC, which maintains a processor queue for each**

processor in the system, then queues the packet descriptor to the appropriate processor queue based on the hash value, (Kaniyar et al., Paragraph 10, Page 2)].

Regarding claim 32, a method wherein said supported service profile is used as additional selection criteria, **[If the data packet is not of the type that should be scaled, in step 508, the selected processor is chosen based on other load-balancing criteria, (Kaniyar et al., Paragraph 40, Page 5)].**

Regarding claim 33, a method wherein said load balancer is configured to obtain a load state from each processor upon a hardware based mechanism, **[A suitable hardware structure for achieving scalability beyond a single processor is a "symmetric multiprocessor" (SMP) system, (Kaniyar et al., Paragraph 26, Page 3)].**

Regarding claim 34, a method wherein said load balancer is configured to obtain a load state from each processor upon a packet based mechanism, **[After the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests, wherein before choosing one of the processors to handle a request as shown in Fig. 3a, the load-balancing multiprocessor will obtain a connection state of the processors and the**

load state of the processors to send the request to the connected and least busy processor, (Kaniyar et al., Paragraph 31, Page 3)].

Regarding claim 35, Kaniyar et al. teaches implementing symmetrical multiprocessing in a multiprocessor system and increasing performance of the multiprocessor system, **(Kaniyar et al., Paragraph 7, Page 1)**,

Kaniyar et al. fails to teach that the load state of processor is inserted into a packet processed by said processor,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 36, a method wherein a packet returned by a processor is interpreted as a flag for a free resource, **[If the interrupt is disabled, the method returns to step 700 to receive additional data packets and begin the process of storing them, (Kaniyar et al., Paragraph 43, Page 5)].**

Regarding claim 37, a method wherein excess traffic is redirected to another load balancer, said excess traffic being defined upon the number of active processors, **[directing the received data packet to the selected processor; and processing the data packet, (Kaniyar et al., Paragraph 50, Page 7)].**

Regarding claim 41, an apparatus, comprising: selection circuitry configured to select on a per received packet basis, one of a plurality of processors configured to perform communication in a packet switched connection on the basis of a stored load state of the selected processor in such a manner that a respective next received packet is distributed to the selected processor with a lowest load among said processors irrespective of a specific connection to which this next received packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

Kaniyar et al. fails to teach informing the current connection state to respective processors by inserting data indicating the current connection state into a packet to be distributed, Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 42, an apparatus, wherein a load state of a processor is contained in a table, **[An exemplary processor selection policy includes any acceptable manner of cross-referencing the hash value to a processor in the multiprocessor system, including a processor identification table, (Kaniyar et al., Paragraph 40, Page 5)].**

Regarding claim 43, a method wherein said information about the load state is maintained as a Boolean state, **[it is inherent to use a Boolean value, since it is a**

digital or analog that depends on 1s and 0s, or true and false].

Regarding claim 44, an apparatus wherein a load state of a processor is expressed as value which corresponds to the percentage of load, **[The hashing function yields a hash value that identifies which processor is selected to process the data packet, (Kaniyar et al., Paragraph 9, Page 1)].**

Regarding claim 45, an apparatus, wherein said selection circuitry is configured such that a processor is selected also on the basis of a parameter indicating the service profile supported by a respective processor, **[If the data packet is not of the type that should be scaled, in step 508, the selected processor is chosen based on other load-balancing criteria, (Kaniyar et al., Paragraph 40, Page 5)].**

Regarding claim 46, an apparatus, wherein a load state of a processor is contained in a table, **[An exemplary processor selection policy includes any acceptable manner of cross-referencing the hash value to a processor in the multiprocessor system, including a processor identification table, (Kaniyar et al., Paragraph 40, Page 5)].**

Regarding claim 47, Kaniyar et al. teaches implementing symmetrical multiprocessing in a multiprocessor system and increasing performance of the multiprocessor system, **(Kaniyar et al., Paragraph 7, Page 1)**, Kaniyar et al. fails to teach that the load state of processor is inserted into a received packet processed by said processor,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 49, an apparatus wherein a switch configured to redirect excess traffic to another load balancer, said excess traffic being defined upon the number of active processors, **[directing the received data packet to the selected processor; and processing the data packet, (Kaniyar et al., Paragraph 50, Page 7)].**

Regarding claim 50, Kaniyar et al. teaches a system comprising: obtaining a current connection state as well as a current load state of each of a plurality of processors configured to perform communication in a packet switched connection, **[After the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests, wherein before choosing one of the processors to handle a request as shown in Fig. 3a, the load-balancing multiprocessor will obtain a connection state of the processors and the load state of the processors to send the request to the connected and least busy processor, (Kaniyar et al., Paragraph 31, Page 3)],**

selecting on a per received packet basis, by a load balancer configured to distribute load to said a processors, a processor in such a manner that a respective next packet is distributed to one of said processors having a lowest load irrespective of a specific connection to which this next packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

and maintaining information about the load state of each processor so that said selecting is performed by selecting one of said processors to serve and process a respective received packet based on the load state, **[A scheduling processor in the multiprocessor system, selected by a load-balancing algorithm, reads each data packet and applies a mapping algorithm to portions of the data packet yielding a**

map value, wherein the interrupt request rotates between the available processors on a round-robin basis so that the multiprocessor system will maintain information regarding the load and connection state of the processors, (Kaniyar et al., Paragraph 8, Page 1)],

Kaniyar et al. fails to teach informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 51, Kaniyar et al. teaches a computer program embodied on a computer readable medium, the computer readable medium storing code comprising computer executable instructions configured to perform a method comprising: obtaining a current connection state as well as a current load state of each of a plurality of processors configured to perform communication in a packet switched connection, **[After the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests, wherein before choosing one of the processors to handle a request as shown in Fig. 3a, the load-balancing multiprocessor will obtain a connection state of the processors and the load state of the processors to send the request to the connected and least busy processor, (Kaniyar et al., Paragraph 31, Page 3)],**

selecting on a per received packet basis, by a load balancer configured to distribute load to said a processors, a processor in such a manner that a respective next received packet is distributed to one of said processors having a lowest load irrespective of a specific connection to which a respective received packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

and maintaining information about the load state of each processor so that said selecting is performed by selecting one of said processors to serve and process a respective received packet based on the load state, **[A scheduling processor in the multiprocessor system, selected by a load-balancing algorithm, reads each data packet and applies a mapping algorithm to portions of the data packet yielding a map value, wherein the interrupt request rotates between the available processors on a round-robin basis so that the multiprocessor system will maintain information regarding the load and connection state of the processors, (Kaniyar et al., Paragraph 8, Page 1)],**

Kaniyar et al. fails to teach informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 53, an apparatus, comprising, a load balancer, wherein the load balancer is configured to: obtaining a current connection state as well as a current load state of each of a plurality of processors, **[After the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests, wherein before choosing one of the processors to handle a request as shown in Fig. 3a, the load-balancing multiprocessor will obtain a connection state of the processors and the load state of the processors to send the request to the connected and least busy processor, (Kaniyar et al., Paragraph 31, Page 3)],**

Maintain information about the load state of each of said processors, **[A scheduling processor in the multiprocessor system, selected by a load-balancing algorithm, reads each data packet and applies a mapping algorithm to portions of the data packet yielding a map value, wherein the interrupt request rotates between the available processors on a round-robin basis so that the multiprocessor system will maintain information regarding the load and connection state of the processors, (Kaniyar et al., Paragraph 8, Page 1)],** select on a per received packet basis, a processor having the lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next respective received packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

Kaniyar et al. fails to teach informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 54, an apparatus, comprising: maintaining means for maintaining a load state of each of multiple processors performing a packet switched communication connection, **[A scheduling processor in the multiprocessor system, selected by a load-balancing algorithm, reads each data packet and applies a mapping algorithm to portions of the data packet yielding a map value, wherein the interrupt request rotates between the available processors on a round-robin basis so that the multiprocessor system will maintain information regarding the load and connection state of the processors, (Kaniyar et al., Paragraph 8, Page 1)],**

and selecting means for selecting, on a per received packet basis, one of the processors on the basis of its load state in such a manner that a respective next received packet is distributed to a processor having a lowest load irrespective of a specific connection to which a respective received packet belongs, **[the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, (Kaniyar et al., Paragraph 31, Page 3)],**

Kaniyar et al. fails to teach informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 55, Kaniyar et al. teaches implementing symmetrical multiprocessing in a multiprocessor system and increasing performance of the multiprocessor system, **(Kaniyar et al., Paragraph 7, Page 1)**,

Kaniyar et al. fails to teach that the load state of processor is inserted into a packet processed by said processor,

Aviani et al. teaches maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53)**,

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kaniyar et al. by maintaining connection state data in the data communications device that tracks an amount of extra data inserted into packets exchanged between the first and second computerized devices, **(Aviani et al., Col. 6, lines 40-45)**, in order to adjust the connection information associated with that packet so as to not disrupt or disturb the communication session state maintained by the receiving computer system, **(Aviani et al., Col. 3, lines 49-53).**

Regarding claim 56, an apparatus further comprising means for redirecting excess traffic to another device, wherein said excess traffic is defined upon the number of active processors, **[directing the received data packet to the selected processor; and processing the data packet, (Kaniyar et al., Paragraph 50, Page 7)].**

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaniyar et al. (US 2003/0187914) in view of Aviani et al. (US 6,976,085) and further in view of Reimer et al. (US 2002/0059502)

Regarding claim 48, the modified Kaniyar et al. teaches implementing symmetrical multiprocessing in a multiprocessor system and increasing performance of the multiprocessor system, **(Kaniyar et al., Paragraph 7, Page 1)**,

The modified Kaniyar et al. fails to teach that the processors are comprised of multi core digital signal processing elements having a shared data storage for all cores, whereby said device comprises a first level of load balancing configured to select a digital signal processing means and a second level of load balancing configured to select a single core,

Reimer et al. teaches a multi-core digital signal processor having a shared program memory with conditional write protection, **(Reimer et al., Paragraph 8, Page 1)**, in order to provide write protection of the shared program memory which would prevent the software from being loaded or changed, **(Reimer et al., Paragraph 7),**

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the modified Kaniyar by including a multi-core digital signal processor having a shared program memory with conditional write protection, **(Reimer et al., Paragraph 8, Page 1)**, in order to provide write protection of the shared program memory which would prevent the software from being loaded or changed, **(Reimer et al., Paragraph 7, Page 1).**

Response to Arguments

The Applicant Argues:

That the combination of Kaniyar and Aviani doesn't disclose selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs.

In response, the examiner respectfully submits: Kaniyar et al. teaches after the data packet and data packet descriptor are stored in memory 340, an interrupt request (IRQ) is sent from the NIC 320 to a "scheduling processor," one of the processors 350a, 350b in the multiprocessor system 300 chosen through the use of a load-balancing algorithm for the purpose of handling original requests. Ideally, the scheduling processor chosen by the load-balancing algorithm is the least busy processor in the multiprocessor system 300, as discussed in paragraph 31, wherein after receiving the packet and storing the packet the load balancer will handle the requests and send the request tom the processor that has the lowest load or least busy.

Kaniyar et al. further teaches that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs, wherein in fig. 1 wherein the received packet from the remote computer 110 is sent to the lowest load processor regardless of the connection of the packet. Since the received packet is stored the least busy processor will receive it and process it irrespective of the specific connection to which the received packet belongs.

The Applicant Argues:

That the combination of Kaniyar and Aviani in view of Reimer doesn't disclose that the processors are comprised of multi core digital signal processing elements having a shared data storage for all cores.

In response, the examiner respectfully submits: that Reimer et al. teaches a multi-core digital signal processor having a shared program memory with conditional write protection as discussed in paragraph 8, the motivation to combine Reimer to the combination of Kaniyar and Aviani is to provide write protection of the shared program memory which would prevent the software from being loaded or changed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Shaq Taha** whose telephone number is 571-270-1921. The examiner can normally be reached on 8:30am-5pm Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jeff Pwu** can be reached on 571-272-6798.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/S. T./

Examiner, Art Unit 2446

/Jeffrey Pwu/

Supervisory Patent Examiner, Art Unit 2446